In re Patent Application of
ROCHE ET AL.
Serial No. **10/814,823**
Filed: **MARCH 31, 2004**
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REMARKS

Applicants would like to thank the Examiner for the thorough examination of the present application. Applicants also thank the Examiner for the telephonic interview of October 31, 2007 discussing proposed claim amendments. More particularly, the Examiner indicated that further defining the instructions would define over the prior art. Accordingly, to advance prosecution, the independent claims have been amended to recite the a first instruction group includes a first set of operation codes for accessing the lower memory area, and a second instruction group includes a second set of operation codes different than the first set of operation codes. Support for this amendment may be found in paragraphs 0010, and 0024-0025 of Applicants' specification, for example. No new matter is being added.

I. The Claimed Invention

The present invention, as recited amended independent Claim 1, for example, is directed to a microprocessor comprising a processing unit, and a memory connected to the processing unit and comprising an addressable memory space for a lower memory area and an extended memory area. The microprocessor includes an address bus connecting the processing unit to the memory, and comprising a lower address bus for accessing the lower memory area, and an extended address bus for accessing the extended memory area, and means for executing instructions of an instruction set executable by the processing unit. The instruction set

comprises instructions for accessing a first instruction group
comprising a first set of operation codes for accessing the
lower memory area, and a second instruction group comprising a
second set of operation codes different than the first set of
operation codes for accessing the extended memory area. The
microprocessor also comprises means for forcing to zero an
extended address transmitted by the extended address bus when
executing an instruction in the first instruction group so
that the lower memory area is accessed.

Amended independent Claim 11 further recites a
circuit for forcing to zero an extended address and a set of
instructions executable by the processing unit. Amended
independent Claim 21 is a corresponding method claim of
amended independent Claim 1. Independent Claims 11 and 21 have
been amended similar to amended independent Claim 1.

II. The Claims Are Patentable

The Examiner rejected independent Claims 1, 11, and
21 as being disclosed by Ronen et al. Ronen et al. discloses
an apparatus and methods for porting a 32-bit application to
32-bit address space in a 64-bit processing environment. The
apparatus includes a processing unit, a memory, and a 64-bit
address register. An instruction core receives instructions
from the memory and, when executed, generates an address
reference that includes 64 bits and is stored in the 64-bit
register. When the address space control flag is set, the
instruction core can truncate the 64 bit generated address to
32 bits. If the ported 32-bit application uses a signed

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address space, the generated address reference can be extended up to 64 bits. If the address space is unsigned address space, the truncated generated references can be zero extended to 64 bits. Additionally, a format control flag can specify whether an address is sign extended or zero extended.

Applicants respectfully submit that Ronen et al. fails to disclose a first instruction group comprising a first set of operation codes for accessing the lower memory area, and a second instruction group comprising a second set of operation codes different than the first set of operation codes, as recited in the amended independent claims. Instead, Ronen et al. merely discloses that a same operation instruction can access a 64-bit memory or a truncated 32-bit memory depending on the value of the flag stored in control logic, as agreed during the interview. (See Col. 3, lines 16-54).

Accordingly, it is submitted that amended independent Claims 1, 11 and 21 are patentable over the prior art. In view of the patentability of the amended independent claims, it is submitted that their dependent claims, which include yet further distinguishing features of the invention are also patentable. These dependent claims need no further discussion herein.
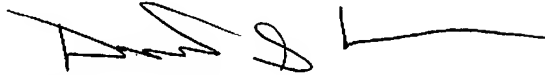
III. CONCLUSION

In view of the arguments provided herein, it is submitted that all the claims are patentable. Accordingly, a Notice of Allowance is requested in due course. Should any

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minor informalities need to be addressed, the Examiner is encouraged to contact the undersigned attorney at the telephone number listed below.

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